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Reg. No. : .....

Name : .....

Fourth Semester B.Tech. Degree Examination, July 2015
(2008 Scheme)
08.402 – DIGITAL ELECTRONICS AND LOGIC DESIGN (E)

Time : 3 Hours Max. Marks : 100

Instructions : *Answer **all** questions from 'Part **A**' and **three** full questions from 'Part **B**' not choosing more than **one** question from **each** Module.*

PART – A

1. Differentiate between straight binary and gray code.
2. State De-Morgan's theorems and explain.
3. Perform the following BCD addition
   i) 1001 + 0100
   ii) 01100111 + 01010011
4. Compare TTL and CMOS logic families.
5. Implement the following function using a multiplexer $f(A.B.C) = \sum(1,3,5,6)$.
6. Give the truth table and draw the logic circuit of a 4 bit (including parity) odd parity generator.
7. What is race around condition in flip flops ? How it can be rectified ?
8. Differentiate between synchronous and asynchronous counters.
9. Discuss the applications of shift registers.
10. Distinguish between static and dynamic RAM. **(4×10=40 Marks)**

P.T.O.

PART – B

Module – I

11. a) Perform the following conversions.
    i) Binary number 110010 to Gray code.
    ii) 67.468_{10} to Hexadecimal.
    iii) $ABCD_{16}$ to octal.
    iv) 327.89_{10} to BCD code. **10**

    b) Perform
    i) 7BA + 6C in Hexadecimal.
    ii) – 91 + 16 using 2's complement method. **5**

    c) Explain weighted and unweighted codes. **5**

12. a) Find the minimal POS expression for
    $F(A, B, C, D) = \pi (1, 4, 5, 6, 11, 12, 13, 14, 15)$ and implement the same using NOR gates. **10**

    b) Obtain the canonical SOP and POS expression for the function.
    $f(A, B, C, D) = ABC + A\bar{B}CD + \bar{A}B\bar{C}D + ACD$. **10**

Module – II

13. a) Design and explain a BCD to 7 segment decoder. **10**

    b) Design and realise a gray code to binary code converter. **10**

14. a) Design and realise a 2-bit magnitude comparator. **10**

    b) Draw the logic diagram for implementing a 4 to 16 line decoder from 3 to 8 line decoders. **6**

    c) Distinguish between decoder and demultiplexer. **4**

Module – III

15. a) Design and draw the circuit of a mod-3 synchronous counter using J-K and explain its operation. **10**

    b) Explain the internal diagram of 555 IC and describe its working as a monostable multivibrator. **10**

16. a) Draw the circuit of a 3-bit binary up-down counter and explain its operation. **10**

    b) What is a ripple counter ? Explain how it differs from ring counter with circuit diagrams. **10**